

IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method for processing an information based on a sequence of instructions in an apparatus for data processing, said method comprising the acts of:

detecting a repeated sub-sequence in said sequence of instructions by the apparatus for data processing;

detecting a number of external processing units connected to ports of the apparatus, the external processing units being external to the apparatus;

providing an index information indicating the repetition frequency of said repeated sub-sequence, wherein said index information comprises an integer number set in proportion with a ranking of said repetition rate of said repeated sub-sequence

compared to the repetition rate of other detected repeated sub-sequences; and

determining an allocation between ~~a processing resource~~ the external processing units and said repeated sub-sequence based on said index information.

2. (Previously Presented) The method of claim 1, including generating an instruction containing said index information, and adding said instruction to said sequence of instructions.

Claim 3 (Canceled)

4. (Currently Amended) The method of claim 1, wherein said allocation is determined by comparing said integer number with the number of ~~available processing resources~~ the external processing units.

5. (Currently Amended) The method of claim 4, wherein all repeated sub-sequences for which said integer number is smaller

than said number of ~~available processing resources~~ the external processing units are allocated to a selected processing resource.

6. (Previously Presented) The method of claim 1, wherein said index information comprises an information indicating the number of instructions in said repeated sub-sequence.

7. (Previously Presented) The method of claim 1, including generating an instruction for deleting said repeated sub-sequence, if said repeated sub-sequence is no longer detected for a predetermined time period, and resetting a processing unit to which said deleted repeated sub-sequence was allocated.

8. (Previously Presented) The method of claim 1, including generating an instruction for specifying processing registers used by said repeated sub-sequence, and using said instruction for locking said specified processing registers.

9. (Currently Amended) The method of claim 2, including

activating a ~~processing resource~~ an external processing unit of the external processing units when said instruction containing said index information indicates that the corresponding repeated sub-sequence has already been allocated to said ~~processing resource~~ external processing unit.

10. (Currently Amended) The method of claim 9, wherein said activating comprises programming said ~~processing resource~~ external processing unit according to said corresponding repeated sub-sequence, or uploading said corresponding repeated sub-sequence to a memory of said ~~processing resource~~ external processing unit.

11. (Currently Amended) The method of claim 1, including signalling ~~the presence of~~ the external processing units to a central processing unit, and counting the number of available external processing units based on said signalling.

12. (Currently Amended) An apparatus for processing an information based on a sequence of instructions, said apparatus

comprising a processor configured to:

~~detecting means for detecting~~ detect a repeated sub-sequence in said sequence of instructions, and for providing an index information indicating the repetition frequency of said repeated sub-sequence, wherein said index information comprises an integer number set in proportion with a ranking of said repetition rate of said repeated sub-sequence compared to the repetition rate of other detected repeated sub-sequences; and

~~resource control means for allocating~~ allocate said repeated sub-sequence to a processing resource based on said index information.

13. (Currently Amended) The apparatus of claim 12, further comprising ~~connecting means~~ ports for connecting ~~at least one the~~ external processing ~~unit~~ units to which said repeated sub-sequence can be allocated.

14. (Previously Presented) The apparatus of claim 13, further comprising a memory table for storing an allocation information

indicating an allocation between said at least one external processing unit and corresponding repeated sub-sequences.

15. (Previously Presented) The apparatus of claim 13, wherein said apparatus is a digital signal processor and said at least one external processing units are processor cores and/or configurable logic blocks.

16. (Currently Amended) The apparatus of claim 13, ~~further comprising means for determining wherein the processor is further~~ configured to determine the number of said at least one external processing units connected to said ~~connecting means~~ ports.

17. (Currently Amended) The apparatus of claim 13, ~~further comprising mapping means for mapping wherein the processor is~~ further configured to map said repeated sub-sequence to an available one of said at least one external processing unit based on said index information.

18. (Previously Presented) A compiler stored on a computer readable medium, the compiler for providing an output sequence of instructions to be used for processing an information in an apparatus for data processing, said compiler being arranged to detect a repeated sub-sequence in said output sequence of instructions and to provide an index information indicating the repetition frequency of said repeated sub-sequence, wherein said index information comprises an integer number set in proportion with a ranking of said repetition rate of said repeated sub-sequence compared to the repetition rate of other detected repeated sub-sequences.

19. (Currently Amended) A compiler stored on a computer readable medium, the compiler for providing an output sequence of instructions to be used for processing an information in an apparatus for data processing, said compiler being arranged to detect a repeated sub-sequence in said output sequence of instructions and to provide an index information indicating the repetition frequency of said repeated sub-sequence, wherein said

compiler is arranged to add to said repeated sub-sequence an  
additional instruction specifying said index information.

20. (Previously Presented) The compiler of claim 19, wherein said additional instruction is added so as to precede said repeated sub-sequence.

21. (Previously Presented) A compiler stored on a computer readable medium, the compiler for providing an output sequence of instructions to be used for processing an information in an apparatus for data processing, said compiler being arranged to detect a repeated sub-sequence in said output sequence of instructions and to provide an index information indicating the repetition frequency of said repeated sub-sequence, wherein said compiler is arranged to add to said output sequence an instruction for indicating that said repeated sub-sequence is not used anymore.

22. (Currently Amended) The compiler of claim 18, wherein said compiler is arranged to add to said output sequence an instruction



for allocating at least one processing register means-until said repeated sub-sequence is finished.

23. (Previously Presented) The compiler of claim 18, wherein said compiler is arranged to determine the ranking of repeated sub-sequences based on their repetition rate.

24. (Previously Presented) The compiler of claim 19, wherein said compiler is arranged to allocate said repeated sub-sequence to a separate processing unit.

25. (Previously Presented) The compiler of claim 19, wherein said compiler is arranged to add an additional instruction to said repeated sub-sequence for use in processing notification at execution time.